

**UNITED STATES PATENT APPLICATION**

**OF**

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**FOR**

**ISOLATED FINFET P-CHANNEL/N-CHANNEL  
TRANSISTOR PAIR**

ISOLATED FINFET P-CHANNEL/N-CHANNEL  
TRANSISTOR PAIR

FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor manufacturing and, more particularly, to forming FinFET devices.

BACKGROUND OF THE INVENTION

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET

structure may also be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

#### SUMMARY OF THE INVENTION

**[0005]** Implementations consistent with the principles of the invention merge N-channel and P-channel FinFET devices on a single fin structure. As a result, a maximum density for complimentary FinFET structures can be achieved.

**[0006]** In accordance with the purpose of this invention as embodied and broadly described herein, a semiconductor device includes a fin structure that includes a semiconducting material and a channel stop layer. The semiconductor device further includes a source region formed at one end of the fin structure, the channel stop layer separating the source region into a first source region and second source region. The semiconductor device also includes a drain region formed at an opposite end of the fin structure, the channel stop layer separating the drain region into a first drain region and second drain region. The semiconductor device further includes at least one gate.

**[0007]** In another implementation consistent with the present invention, a semiconductor device includes a fin structure that includes a retrograde channel stop layer that extends a length of the fin structure and positioned approximately in a center of the fin structure. The semiconductor device further includes a source region formed at one end of the fin structure, the retrograde channel stop layer separating the source region into a first source region and second source region. The semiconductor device also includes a drain region formed at an opposite end of the fin structure, the retrograde channel stop layer separating the drain region into a first drain region and second drain region.

**[0008]** In yet another implementation consistent with the principles of the invention, a semiconductor device includes an N-channel device including a first source region, a first drain region, a first fin structure, and a gate. The semiconductor device further includes a P-channel device including a second source region, a second drain region, a second fin structure. The gate, the second source region, the second drain region, and the second fin structure are separated from the first source region, the first drain region, and the first fin structure by a channel stop layer.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

**[0010]** FIGS. 1-10 illustrate exemplary views of a merged N-channel/P-channel FinFET device fabrication process consistent with the principles of the invention; and

**[0011]** FIGS. 11-12 illustrate exemplary views of a stacked fin fabrication process according to an alternative implementation consistent with the principles of the invention.

#### DETAILED DESCRIPTION

**[0012]** The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

**[0013]** Implementations consistent with the principles of the invention form multiple transistors in small amounts of space to achieve increased transistor density.

## EXEMPLARY PROCESSING

[0014] Fig. 1 illustrates an exemplary semiconductor device 100 that includes a silicon-on-insulator (SOI) structure having a silicon substrate 110, a buried oxide layer 120, and a silicon layer 130 on buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

[0015] In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1500 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 200 Å to about 1000 Å. Silicon layer 130 may be used to form a fin structure, as described in more detail below.

[0016] In alternative implementations consistent with the present invention, substrate 110 and layer 130 may comprise other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

[0017] , A retrograde channel stop layer 210 may be implanted into layer 130, as illustrated in FIG. 2. Retrograde channel stop layer 210 may include ions implanted at selected concentrations and implantation energy levels. In one implementation, for example, Boron or Phosphorus Ions having a selected concentration in the range of  $10^{16}$ - $10^{17}$  ions per  $\text{cm}^2$  may be implanted at a selected implantation energy in the range of 5-40 KeV. Retrograde channel stop layer creates a retrograde channel profile in which the peak concentration of implanted ions is below the surface. The retrograde channel concentration profile of channel stop layer 210 may confine a depletion region of a P/N junction that may be formed between a portion of layer 130

on one side of channel stop 210 and a portion of layer 130 on another side of channel stop layer 210.

**[0018]** A photoresist material may be deposited and patterned to form a photoresist mask 310, as illustrated in FIG. 3. The photoresist material may be deposited and patterned in any conventional manner. Semiconductor device 100 may then be etched to form a fin structure 410, as illustrated in FIGS. 4A & 4B. In an exemplary implementation, silicon layer 130 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120. The portion of silicon layer 130 located under photoresist mask 310 will not be etched, thereby, forming a fin structure 410 comprising silicon. In exemplary implementations, the width of fin structure 310 may range from about 70 Å to about 80 Å. In one implementation, the width of fin structure 310 may be approximately 75 Å.

**[0019]** After the formation of fin structure 410, source and drain regions may be formed adjacent the respective ends of fin structure 410. For example, in an exemplary implementation, a layer of silicon, germanium or combination of silicon and germanium may be deposited, patterned and etched in a conventional manner to form source and drain regions. Alternatively, silicon layer 130 may be patterned and etched to form source and drain regions. Fig. 4B illustrates an exemplary top view of semiconductor device 100 including source region 420 and drain region 430 formed adjacent fin structure 410 on buried oxide layer 120. The buried oxide layer and the photoresist mask are not illustrated in Fig. 4B for simplicity.

**[0020]** Photoresist mask 310 may then be removed, as shown in FIG. 5, and a dielectric layer 510 may be formed in a conventional manner over fin structure 410. In one implementation, for example, an oxide (or other material) may be deposited over fin structure

410 to form dielectric layer 510. The thickness of dielectric layer 510 may range from about 50 Å to about 300 Å.

**[0021]** A photoresist material may be deposited and patterned to form another photoresist mask 520, as illustrated in FIG. 5. The photoresist material may be deposited and patterned in any conventional manner. Dielectric layer 510 may then be etched to form a gate dielectric 610 around portions of fin structure 410, as illustrated in FIG. 6. In one implementation, dielectric layer 510 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120. The portion of dielectric layer 510 located under photoresist mask 520 will not be etched, thereby, forming gate dielectric 610. In exemplary implementations, the thickness of gate dielectric 610 may range from about 50 Å to about 300 Å.

**[0022]** A layer of material may then be deposited and etched to form one or more gate electrodes 710, and one or more contacts 760, as illustrated in FIGS. 7A and 7B. In an exemplary implementation, the layer of material may include polysilicon deposited using conventional chemical vapor deposition (CVD) to a thickness ranging from about 200 Å to about 500 Å. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material. In one implementation, the layer of material may be patterned and etched to form one or more gate electrodes 710 that surround top and side surfaces of fin structure 410, and one or more contacts 760 that contact side surfaces of fin structure 410.

**[0023]** As illustrated in FIG. 7A, retrograde channel stop layer 210 causes two separate source regions 720 and 740 to be formed, along with two separate drain regions 730 and 750. In this way, an N-channel transistor device can be formed on one side of retrograde channel stop

layer 210 (e.g., including source region 740 and drain region 750) and a P-channel transistor device can be formed on the opposite side of retrograde channel stop layer 210 (e.g., including source region 720 and drain region 730). Fig. 7B illustrates an exemplary three-dimensional view of semiconductor device 100 of Fig. 7A. The view illustrated in Fig. 7B is taken along line BB in FIG. 7A.

**[0024]** Source/drain regions 720, 730, 740, and 750 may then be doped with n-type or p-type impurities based on the particular end device requirements. In exemplary implementations consistent with the principles of the invention, source region 720 and drain region 730 of the P-channel device may be doped with p-type impurities and source region 740 and drain region 750 of the N-channel device may be doped with n-type impurities.

**[0025]** For example, a conventional implant process of n-type impurities, such as arsenic or phosphorus, may be performed to dope source region 740 and drain region 750, as illustrated in FIG. 8. The n-type impurities 810 may be implanted at a tilt angle ranging from approximately 10 degrees to 80 degrees. In an exemplary implementation, the implant process may be performed at an angle of approximately 30 degrees. Using a tilt angle ensures that source and drain regions 720 and 730 will not be doped during this first ion implantation process.

**[0026]** In an exemplary implementation, phosphorus may be implanted at a dosage of about  $5 \times 10^{14}$  atoms/cm<sup>2</sup> to about  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and an implantation energy of about 3 KeV to about 6 KeV, which may depend on the thickness of source region 740 and drain region 750 and the desired junction depths for source/drain regions 740 and 750. In an alternative implementation, arsenic may be implanted at a dosage of about  $5 \times 10^{14}$  atoms/cm<sup>2</sup> to about  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and an implantation energy of about 5 KeV to about 10 KeV, which may

depend on the thickness of source region 740 and drain region 750 and the desired junction depths for source/drain regions 740 and 750.

**[0027]** A tilt angle implant process of p-type impurities, such as boron or  $\text{BF}_2$ , may be performed to dope source region 720 and drain region 730, as further illustrated in FIG. 8. The p-type impurities 820 may be implanted at an angle ranging from approximately 10 degrees to 80 degrees. In an exemplary implementation, the implant process may be performed at an angle of approximately 30 degrees.

**[0028]** The p-type impurities 820 may be implanted at a dosage of about  $5 \times 10^{14}$  atoms/cm<sup>2</sup> to about  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and an implantation energy of about 2 KeV to about 3 KeV, which may depend on the thickness of source region 720 and drain region 730 and the desired junction depths for source/drain regions 720 and 730. The above implant processes may alter the work function of gate 710 in the N-channel region and the P-channel region to achieve desirable threshold voltages for the resulting N-channel and P-channel devices. Channel stop layer 210 may further create a retrograde channel concentration profile that confines a depletion region of the P/N junction formed between the P-channel of source/drain regions 720 and 730 and the N-channel of source/drain regions 740 and 750. Control of the depletion region between the P-channel and the N-channel devices results in forward diode isolation between the channels, thus, preventing a short.

**[0029]** It will be appreciated that sidewall spacers may optionally be formed prior to the source/drain ion implantation processes described above to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate source/drain regions 720/730 and 740/750.

**[0030]** As a result of the above processing, an N-channel/P-channel transistor pair may be formed, having a common gate 710 and independent source regions 720 and 740 and drain regions 730 and 750. As illustrated in FIG. 9, the polysilicon may also be selectively removed from contacts 760 in the source region of semiconductor device 100. Once the polysilicon is selectively removed, a polysilicon contact 760 may be formed on both sides of semiconductor device 100 in the source region. A self-aligned silicide (salicide) process may then be performed for contact 760. For example, a metal may be deposited on contact 760, followed by an annealing to form a metal-silicide layer on contact 760. As further shown in FIG. 10, an interconnect 1010 may be further be formed with gate 710.

**[0031]** Fig. 11 illustrates a view of an exemplary semiconductor device 1100 that includes a silicon-on-insulator (SOI) structure having a silicon substrate 1110, a buried oxide layer 1120, a first semiconducting layer 1130 on buried oxide layer 1120, an insulating layer 1140, and a second semiconducting layer 1150. Buried oxide layer 1120, semiconducting layers 1130 and 1150, and insulating layer 1140 may be formed on substrate 1110 in a conventional manner.

**[0032]** In an exemplary implementation, buried oxide layer 1120 may include silicon oxide and may have a thickness ranging from about 1500 Å to about 3000 Å. Semiconducting layer 1130 may include monocrystalline or polycrystalline silicon having a thickness of  $t_N$ . Semiconducting layer 1150 may include monocrystalline or polycrystalline silicon having a thickness of  $t_P$ , where  $t_N \neq t_P$ . Insulating layer 1140 may include, for example, any dielectric material that will insulate layers 1130 and 1150 from one another. Layers 1130, 1140 and 1150 may be used to form a fin structure, as described in more detail below.

**[0033]** In alternative implementations consistent with the present invention, substrate 1110 and layers 1130 and 1150 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 1120 may also include other dielectric materials.

**[0034]** As shown in FIG. 12, semiconductor device 1100 may be etched, for example, to form a fin structure 1210 from layers 1130, 1140 and 1150. Fin structure 1210 may include a first channel 1220 and a second channel 1230. The first channel 1220 may include, for example, a N-channel and the second channel 1230 may include, for example, a P-channel. The relative heights (i.e., thicknesses) of the first channel 1220 versus the second channel 1230 may be selected to set the P/N junction drain saturation current ( $I_{DSAT}$ ) ratio. The drain saturation current ratio may, thus, be controlled in a variable fashion by the relative thicknesses ( $t_N$  &  $t_P$ ) of the first 1220 and second 1230 channels. In some implementations, for example, the thicknesses of first channel 1220 and second channel 1230 may be selected such that the current for each channel is matched. Subsequent to formation of fin structure 1210, a FinFET gate (not shown) may then be formed, in a conventional manner, over fin structure 1210 to create a FinFET transistor.

## CONCLUSION

**[0035]** Implementations consistent with the principles of the invention merge N-channel and P-channel FinFET devices on a single fin structure. As a result, increased density for complimentary FinFET structures can be achieved.

**[0036]** The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the

above teachings or may be acquired from practice of the invention. For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

**[0037]** While a series of acts has been described with respect to FIGS. 1-12, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

**[0038]** No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

**[0039]** The scope of the invention is defined by the claims and their equivalents.